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1 Applications of storage mapping optimization to register promotion
Patrick Carribault, Albert Cohen
June 2004 ICS '04: Proceedings of the 18th annual international conference on Supercomputing
Publisher: ACM
Full text available: pdf(268.41 KB) Additional Information: full citation, abstract, references, index terms

Storage mapping optimization is a flexible approach to folding array dimensions in numerical codes. It is designed to reduce the memory footprint after a wide spectrum of loop transformations, whether based on uniform dependence vectors or more expressive ...

Keywords: array contraction, array folding, blocking, itanium, pattern matching, register promotion, scheduling, string matching, tiling

2 VLIW instruction scheduling for minimal power variation
Shu Xiao, Edmund M.-K. Lai
September 2007 ACM Transactions on Architecture and Code Optimization (TACO), Volume 4 Issue 3
Publisher: ACM
Full text available: pdf(796.99 KB) Additional Information: full citation, abstract, references, index terms

The focus of this paper is on the minimization of the variation in power consumed by a VLIW processor during the execution of a target program through instruction scheduling. The problem is formulated as a mixed-integer program (MIP) and a problem-specific ...

Keywords: Instruction scheduling, VLIW processors, power variation reduction

3 Efficient instruction scheduling for delayed-load architectures
Steven M. Kurlander, Todd A. Proebsting, Charles N. Fischer
September 1995 ACM Transactions on Programming Languages and Systems (TOPLAS), Volume 17 Issue 5
Publisher: ACM
Full text available: pdf(2.30 MB) Additional Information: full citation, abstract, references, cited by, index terms, review

A fast, optimal code-scheduling algorithm for processors with a delayed load of one instruction cycle is described. The algorithm minimizes both execution time and register use and runs in time proportional to the size of the expression-tree. An extension ...

4 Register allocation for irregular architectures

Bernhard Scholz, Erik Eckstein
June 2002 LCTES/ SCOPES '02: Proceedings of the joint conference on Languages, compilers and tools for embedded systems: software and compilers for embedded systems
Publisher: ACM

Full text available: pdf(220.34 KB) Additional Information: full citation, abstract, references, cited by, index terms

For irregular architectures global register allocation is still a challenging problem that has not been successfully solved so far. The graph-coloring analogy of traditional approaches does not match the needs of register allocation for such architectures ...

Keywords: boolean quadratic problem, register allocation

5 An efficient technique for exploring register file size in ASIP synthesis
Manoj Kumar Jain, M. Balakrishnan, Anshul Kumar
October 2002 CASES '02: Proceedings of the 2002 international conference on Compilers, architecture, and synthesis for embedded systems
Publisher: ACM

Full text available: pdf(244.85 KB) Additional Information: full citation, abstract, references, cited by, index terms

Performance estimation is a crucial operation which drives the design space exploration in Application Specific Instruction Set Processors (ASIP) synthesis. The usual approach to estimate performance is to do simulation. With increasing dimensions of ...

Keywords: ASIP Synthesis, design space exploration, global analysis, instruction scheduling, liveness analysis, register file, register spill, retargetable estimation, storage exploration

6 A general framework to build new CPUs by mapping abstract machine code to instruction level parallel execution hardware
H. C. Wang, C. K. Yuen
November 2005 ACM SIGARCH Computer Architecture News, Volume 33 Issue 4
Publisher: ACM

Full text available: pdf(368.21 KB) Additional Information: full citation, abstract, references, index terms

Abstract machines bridge the gap between a programming language and real machines. This paper proposes a general purpose tagged execution framework that may be used to construct a CPU. The CPU may accept code written in any (abstract or real) machine ...

7 Vector instruction set support for conditional operations
J. E. Smith, Greg Faanes, Rabin Sugumar
May 2000 ACM SIGARCH Computer Architecture News, Volume 28 Issue 2
Publisher: ACM

Full text available: pdf(69.34 KB) Additional Information: full citation, abstract, references, cited by, index terms

Vector instruction sets are receiving renewed interest because of their applicability to multimedia. Current multimedia instruction sets use short vectors with SIMD implementations, but long vector, pipelined implementations have a number of advantages ...

8 Inferring annotated types for inter-procedural register allocation with constructor flattening
Torben Amtoft, Robert Muller

January 2003 TLDI '03: Proceedings of the 2003 ACM SIGPLAN international workshop on Types in languages design and implementation
Publisher: ACM
Full text available: pdf(268.82 KB) Additional Information: full citation, abstract, references, index terms

We introduce an annotated type system for a compiler intermediate language. The type system is designed to support inter-procedural register allocation and the representation of tuples and variants directly in the register file. We present an algorithm ...

Keywords: certifying compilers, defunctionalization, effects, register allocation, type systems

9 Instruction scheduling for a tiled dataflow architecture
Martha Mercaldi, Steven Swanson, Andrew Petersen, Andrew Putnam, Andrew Schwerin, Mark Oskin, Susan J. Eggers
October 2006 ACM SIGOPS Operating Systems Review, Volume 40 Issue 5
Publisher: ACM
Full text available: pdf(490.59 KB) Additional Information: full citation, abstract, references, cited by, index terms

This paper explores hierarchical instruction scheduling for a tiled processor. Our results show that at the top level of the hierarchy, a simple profile-driven algorithm effectively minimizes operand latency. After this schedule has been partitioned ...

Keywords: dataflow, instruction scheduling, tiled architectures

10 On the Complexity of Register Coalescing
Florent Bouchez, Alain Darte, Fabrice Rastello
March 2007 CGO '07: Proceedings of the International Symposium on Code Generation and Optimization
Publisher: IEEE Computer Society
Full text available: pdf(277.05 KB) Additional Information: full citation, abstract, index terms

Memory transfers are becoming more important to optimize, for both performance and power consumption. With this goal in mind, new register allocation schemes are developed, which revisit not only the spilling problem but also the coalescing problem. ...

11 Spill-free parallel scheduling of basic blocks
B. Natarajan, M. Schlansker
December 1995 MICRO 28: Proceedings of the 28th annual international symposium on Microarchitecture
Publisher: IEEE Computer Society Press
Full text available: pdf(684.00 KB) Additional Information: full citation, references, cited by, index terms

12 An optimistic and conservative register assignment heuristic for chordal graphs
Philip Brisk, Ajay Kumar Verma, Paolo Ienne
September 2007 CASES '07: Proceedings of the 2007 international conference on Compilers, architecture, and synthesis for embedded systems
Publisher: ACM
Full text available: pdf(342.34 KB) Additional Information: full citation, abstract, references, index terms

This paper presents a new register assignment heuristic for procedures in SSA Form, whose interference graphs are chordal; the heuristic is called optimistic chordal coloring (OCC). Previous register assignment heuristics eliminate copy instructions ...

Keywords: chordal graph, register assignment, static single assignment (ssa) form

13 Scientific Computations on Modern Parallel Vector Systems
Leonid Oliker, Andrew Canning, Jonathan Carter, John Shalf, Stephane Ethier
November 2004 SC '04: Proceedings of the 2004 ACM/IEEE conference on Supercomputing
Publisher: IEEE Computer Society
Full text available: pdf(239.19 KB) Additional Information: full citation, abstract, references, cited by

Computational scientists have seen a frustrating trend of stagnating application performance despite dramatic increases in the claimed peak capability of high performance computing systems. This trend has been widely attributed to the use of superscalar-based ...

14 Optimistic coalescing for heterogeneous register architectures
Minwook Ahn, Jooyeon Lee, Yunheung Paek
June 2007 LCTES '07: Proceedings of the 2007 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools
Publisher: ACM
Full text available: pdf(656.33 KB) Additional Information: full citation, abstract, references, index terms

In this paper, Optimistic coalescing has been proven as an elegant and effective technique that provides better chances of safely coloring more registers in register allocation than other coalescing techniques. Its algorithm originally assumes *homogeneous* ...

Keywords: compiler, embedded processors, heterogeneous register architecture, register allocation, register coalesing

15 Two-level hierarchical register file organization for VLIW processors
Javier Zalamea, Josep Llosa, Eduard Ayguadé, Mateo Valero
December 2000 MICRO 33: Proceedings of the 33rd annual ACM/IEEE international symposium on Microarchitecture
Publisher: ACM
Full text available: pdf(154.90 KB) ps(843.85 KB) Publisher Site Additional Information: full citation, references, cited by, index terms

16 Improved spill code generation for software pipelined loops
Javier Zalamea, Josep Llosa, Eduard Ayguadé, Mateo Valero
May 2000 ACM SIGPLAN Notices, Volume 35 Issue 5
Publisher: ACM
Full text available: pdf(688.06 KB) Additional Information: full citation, abstract, references, cited by, index terms

Software pipelining is a loop scheduling technique that extracts parallelism out of loops by overlapping the execution of several consecutive iterations. Due to the overlapping of iterations, schedules impose high register requirements during their ...

Keywords: instruction-level parallelism, register allocation, software pipelining, spill code

17 Efficient register and memory assignment for non-orthogonal architectures via graph coloring and MST algorithms
Jeonghun Cho, Yunheung Paek, David Whalley
June 2002 LCTES/SCOPES '02: Proceedings of the joint conference on Languages, compilers

and tools for embedded systems: software and compilers for embedded systems
Publisher: ACM

Full text available: pdf(198.37 KB) Additional Information: full citation, abstract, references, cited by, index terms

Finding an optimal assignment of program variables into registers and memory is prohibitively difficult in code generation for *application specific instruction-set processors* (ASIPs). This is mainly because, in order to meet stringent speed and ...

Keywords: compiler, dual memory, graph coloring, maximum spanning tree, memory assignment, non-orthogonal architecture

18 A retargetable register allocation framework for embedded processors

Jean-Marc Daveau, Thomas Thery, Thierry Lepley, Miguel Santana
June 2004 LCTES '04: Proceedings of the 2004 ACM SIGPLAN/SIGBED conference on Languages, compilers, and tools for embedded systems
Publisher: ACM

Full text available: pdf(1.03 MB) Additional Information: full citation, abstract, references, cited by, index terms

This paper describes the FlexCC2 register allocation framework. FlexCC2 is an optimizing retargetable C compiler for embedded processors, and in particular for DSP processors. Embedded processors often contain features such as irregular and constrained ...

Keywords: embedded processors, register allocation

19 Instruction scheduling for a tiled dataflow architecture

Martha Mercaldi, Steven Swanson, Andrew Petersen, Andrew Putnam, Andrew Schwerin, Mark Oskin, Susan J. Eggers
November 2006 ACM SIGPLAN Notices, Volume 41 Issue 11
Publisher: ACM

Full text available: pdf(490.50 KB) Additional Information: full citation, abstract, references, cited by, index terms

This paper explores hierarchical instruction scheduling for a tiled processor. Our results show that at the top level of the hierarchy, a simple profile-driven algorithm effectively minimizes operand latency. After this schedule has been partitioned ...

Keywords: dataflow, instruction scheduling, tiled architectures

20 Instruction scheduling for a tiled dataflow architecture

Martha Mercaldi, Steven Swanson, Andrew Petersen, Andrew Putnam, Andrew Schwerin, Mark Oskin, Susan J. Eggers
October 2006 ASPLOS-XII: Proceedings of the 12th international conference on Architectural support for programming languages and operating systems
Publisher: ACM

Full text available: pdf(490.50 KB) Additional Information: full citation, abstract, references, cited by, index terms

This paper explores hierarchical instruction scheduling for a tiled processor. Our results show that at the top level of the hierarchy, a simple profile-driven algorithm effectively minimizes operand latency. After this schedule has been partitioned ...

Keywords: dataflow, instruction scheduling, tiled architectures